REMARKS

In the application, claims 24-46 are pending. In the Office action, claims 24-46 are rejected.

In response to the final Office Action of December 11, 2007, Applicant has amended claims 24, 41, 42, and 45 to more clearly define the feature of sole accessing the data. Within the sole addressing, the data within all of the at least two memories is accessed through control and address ports of only one of the terminals. Furthermore, the data within all of the at least two memory areas is provided through data ports of both of the terminals. By this, it is made clear that in case of sole addressing, no distinction is made between certain locations within the memory areas. All locations within the memory areas are accessible through control and address ports of one terminal and data stored within the accessible areas is provided through data ports of both terminals. Support for this amendment is found in the original application as filed, including Figure 2 and in the specification, including page 2, line 25 through page 7, line 17 and page 10, line 16 through page 11, line 16. No new matter has been introduced by way of amendment.

35 U.S.C. 103(a) Rejections

At sections 2-22 of the Office action, the Office rejects claims 24-46 under 35 U.S.C. 103(a) as being unpatentable over *Camacho et al.* (U.S. 6,167,487, hereafter referred to as *Camacho*) in view of *Ware et al.* (U.S. 6,826,657, hereafter referred to as *Ware*). Of these claims, claims 24, 41-42 and 45 are independent. At sections 23-32 of the Office action, the Office presents arguments concerning the prior art rejections. For the reasons set forth below, the Applicant respectfully requests reconsideration of the rejection.

In the Office Action, the Office correctly asserts that the *Camacho* reference does not disclose expressively the case of sole addressing in which the data is provided

through data ports of both terminals. However, the Office is of the opinion that *Ware* discloses this feature. In particular, the Office relies on col. 15, l. 47- col. 16, l. 3, as well as col. 32, l. 16-23, col. 7, l. 6-25. At section 28 of the Office action, the Office asserts that claims 24, 41-42 and 45 recite ""sole addressing... OR individual addressing;" therefore, any prior art of record that meets either sole addressing or individual addressing, meets the claim requirements as the claims require alternatively sole addressing or individual addressing." It is respectfully submitted, however, that any prior art that discloses sole addressing or individual addressing must also disclose or suggest all of the limitations of the disclosed type of addressing (i.e. sole or individual). Applicant respectfully submits that the combination of *Camacho* in view of *Ware* does not disclose all the limitations of sole addressing as claimed.

It is respectfully submitted that the feature of sole addressing and accessing the data, where access controllers provide access to all of the at least two memory areas by control ports and address ports of only one of the terminals and provide the data within both of the two memory areas through data ports of both terminals is not disclosed by *Ware*. According to *Ware* (col. 15, l. 47- col. 16, l. 3), the memory system 150 may comprise a first memory module 160 connected to two ports (1a, 1b) 154, 156 through data busses QDx and QDy.

Access to the memory module 160 may be done in a first mode. Within the first mode, half of the storage locations in the memory components 144 are accessible through the QDx data bus and the other half of the storage locations in the memory components is accessible through the QDy data bus. Thus, in the first mode, one data bus provides access to a first location in the memory components and another data bus provides access to a second location in the memory components. The feature of accessing the data within all of the at least two memory areas through data ports of both terminals is not provided.

Further, as pointed out by the Office at sections 29 and 31 of the Office action, there is a second mode according to *Ware*, within which all of the storage locations are accessible through the QDx data bus, while the QDy data bus is unused. By providing access through all storage locations through only one data bus, different to the teaching of the invention wherein all of the at least two memory areas are accessed through data ports of both terminals, the data bandwidth cannot be increased according to the *Ware* teaching. In particular the second mode, according to the *Ware* teaching, explicitly teaches to disable one of the data busses QDy, or QDx, when accessing all of the storage locations through the respective other data bus QDx, or QDy. Making the respective other data bus inactive reduces the overall bandwidth, by which the areas may be accessed. It must be understood that an advantage provided by the claimed invention is an increase in bandwidth in case of sole addressing, as the whole memory areas can be accessed and data is provided through data ports of both terminals, even though only control ports and address ports of only one terminal are used. This is in direct contrast to that which is disclosed by *Ware* wherein, in the first mode, either one half of the storage locations are accessible through the QDx data bus and the other half are accessible through the QDy data bus, or, in the second mode, all storage locations are accessible through one data bus, and the other data bus is disabled. Neither of the two modes allows accessing all memory areas through control ports and address ports of only one terminal and reading and writing data within all of the at least two memory areas through data ports of both terminals. Consequently, *Ware* does not disclose "wherein in case of sole addressing and accessing the data, the access controllers provide access to all of the at least two memory areas by control ports and address ports of only one of the terminals and provide the data within all of the at least two memory areas through data ports of both terminals," as recited in claim 24. Thus, *Camacho* in view of *Ware* fails to render claim 24 obvious, and therefore Applicant respectfully requests reconsideration and withdrawal of the rejection of claim 24.

Claims 41-42 and 45 are independent claims which contain similar features of claim 24 described above. For at least the reasons presented above

regarding claim 24, claims 41-42 and 45 are also patentable over *Camacho* in view of *Ware*. Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 41-42 and 45.

At section 30 of the Office action, the Office presents arguments with regard to the recited features of dependent claim 38, which depends from independent claim 24. Claims 25-40, 43-44 and 46 are dependent claims and recite features not recited in the independent claims. For the reasons regarding claims 24, 41-42 and 45 above, *Camacho* in view of *Ware* does not render the claimed invention obvious. Therefore, all of the dependent claims are also patentable over the cited art.

CONCLUSION

It is respectfully submitted that the amendments to claims 24, 41-42 and 45 have been made to more distinctly claim the invention and do not raise any new issues, thus are not believed to require any further examination by the Office. As such, entry of this amendment is earnestly solicited.

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance and such action is earnestly solicited.

Respectfully submitted,

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Cathy A. Sturmer
Agent for Applicants
Registration No. 60,869

WARE, FRESSOLA, VAN DER
SLUYS & ADOLPHSON LLP
Building Five, Bradford Green
755 Main Street, P.O. Box 224
Monroe, CT 06468
Telephone: (203) 261-1234
Facsimile: (203) 261-5676
USPTO Customer No. 004955